REMARKS

In the Office Action mailed April 20, 2006, the Examiner rejected claims 1-19 under 35 U.S.C. § 103(a). Applicants have amended claim 1 to clarify that the guard ring extends through the buried oxide layer contacting the semiconductor substrate. No new matter has been added. Applicants submit that claims 1-19 are in condition for allowance and respectfully request notice to this effect.

I. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Hirabayashi

The Examiner rejected claims 1, 2, 5, 6, 9, 10, 13, 14, and 17-19 under 35 U.S.C. § 103(a) as being obvious in view of the combination of U.S. Patent No. 6,429,502 ("Librizzi") and U.S. Patent No. 5,889,314 ("Hirabayashi"). In amended claim 1, Applicants recite an integrated circuit having a semiconductor substrate, a buried insulation layer, a semiconductor mesa, and a guard ring. The guard ring extends through the buried insulation layer contacting the semiconductor substrate. The use of a buried insulation layer provides additional RF isolation. (See, e.g., Applicants' Specification, page 12, lines 11-17.)

Neither Librizzi, nor Hirabayashi teach an integrated circuit having a guard ring as claimed. The Examiner states, and Applicants agree, that Librizzi fails to disclose a guard ring that is in contact with the semiconductor substrate. (Office Action, page 2.) Librizzi's guard ring does not contact the semiconductor substrate because it is formed on the insulation layer. (See, e.g., Librizzi, Fig. 2.) Thus, Librizzi does not show or suggest a guard ring that extends through the buried insulation layer contacting the semiconductor substrate.

While Hirabayashi describes a guard ring that contacts the semiconductor substrate, Hirabayashi's guard ring does not extend through a buried insulation layer. Instead, Hirabayashi's guard ring extends through a p-well that formed by implanting a p-type impurity in silicon and heating the silicon to activate the implanted p-type impurity. (See, e.g., Hirabayashi, col. 4, lines 5-9.) Because Hirabayashi's design does not include a buried insulation layer over the semiconductor substrate, Hirabayashi does not show or suggest a guard ring that extends through the buried insulation layer contacting the semiconductor substrate.

Because neither Librizzi nor Hirabayashi show or suggest a guard ring that extends through a buried insulation layer contacting a semiconductor substrate, Applicants submit that claim 1 is not obvious in view of the combination of Librizzi and Hirabayashi. Claims 2, 5, 6, 9, 10, 13, 14, and 17-19 depend from claim 1. Accordingly, Applicants also submit that claims 2, 5, 6, 9, 10, 13, 14, and 17-19 are not obvious in view of the combination of Librizzi and Hirabayashi for at least the reasons described above with reference to claim 1.

In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

II. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Hirabayashi/Beyer

The Examiner rejected claims 3, 4, 7, 8, 11, 12, 15, and 16 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Librizzi, Hirabayashi, and U.S. Patent No. 5,264,387 ("Beyer"). Claims 3, 4, 7, 8, 11, 12, 15, and 16 depend from claim 1. As described above, neither Librizzi nor Hirabayashi show or suggest a guard ring that extends through the buried insulation layer

contacting the semiconductor substrate. The Examiner cited to Beyer for the teaching of a semiconductor device that has a semiconductor mesa that comprises a silicon mesa. (Office Action, page 4.) However, this teaching of Beyer does not overcome the deficiencies identified with respect to Librizzi and Hirabayashi. Accordingly, Applicants submit that claims 3, 4, 7, 8, 11, 12, 15, and 16 are not obvious in light of the combination of Librizzi, Hirabayashi, and Beyer for at least the reasons described above with reference to claim 1.

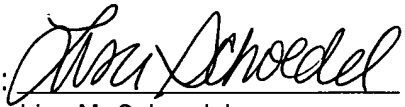
In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

CONCLUSION

In light of the above amendments and remarks, Applicants submit that the present application is in condition for allowance and respectfully request notice to this effect. The Examiner is requested to contact Applicants' representative below if any questions arise or she may be of assistance to the Examiner.

Respectfully submitted,

Date: July 20, 2006

By: 

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